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(71) Applicant: **TOSHIBA CORP**

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(57) Abstract:

PROBLEM TO BE SOLVED: To speed up the operation of an SRAM which adopts a DDR(double data rate) system operation mode by suppressing the delay and variance of the timing of data output or data input.

SOLUTION: The SRAM which adopts the DDR system operation mode is provided with data buses 81 and 82 where data read out of and written to memory cells are propagated, a readout control circuit which performs control so that pieces of data are read out of memory cells corresponding to addresses are read out almost at the same time, output data registers 913 and 914 provided corresponding to the data buses, and a data bus control circuit 21 which optionally controls the connection relation between memory cells and output data registers by controlling the connection relation of the data

buses from the memory cells to the output data registers.